A1

FIG. 2 is a partial perspective view that shows the structure of the semiconductor chip and the conductive bump of the semiconductor package of FIG. 1.

Please replace the paragraph starting on page 3, line 15 with the following replacement paragraph.

A2

Use of the same reference symbols in different drawings indicates similar or identical items.

Please replace the paragraph starting on page 3, line 22 with the following replacement paragraph.

A3

FIG. 1 shows a semiconductor package 100 in accordance with an embodiment of the present invention. In the semiconductor package 100, a semiconductor chip 10, which has conductive bumps 16 on an active surface of the chip 10, is on a substrate 20, such that the conductive bumps 16 connect to bonding pads 22 formed on the substrate 20. The substrate 20 further includes external terminals 21 for electrically connecting the semiconductor chip 100 to an external component. The bonding pads 22 electrically connect to respective external terminals 21 through a circuit pattern (not shown) formed, for example, in the substrate 20. The external terminals 21 can have various forms, such as straight leads, gull-wing type leads, and solder balls. As an example, the external terminals 21 of FIG. 1 are straight leads.

Please replace the paragraph starting on page 4, line 3 with the following replacement paragraph.

A4

Between the chip 10 and the substrate 20, an under-filling portion 50 is formed to prevent cracking of the conductive bumps 16 due to the thermal expansion mismatch between the chip 10 and the substrate 20. Then, in order to promote the heat dissipation from the chip 10, a plate-shaped heat slug 40 is attached on the backside of the chip 10, on which an adhesion layer 14 is formed, using a solder film 30. The heat slug 40 is formed of a metal such as Cu, Al or CuW. In addition, grooves 43 are formed on the heat slug 40 to facilitate the heat dissipation by increasing the surface area of the heat slug 40. In addition, an

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adhesion layer (not shown), which is typically a Ni/Al, Ag, or Pd layer, can be formed on one side 41 of heat slug 40 contacting the solder film 30 to secure the bonding between the heat slug 40 and the conductive solder film 30, and an anodizing layer (not shown) is formed on the other side of the heat slug 40 to prevent oxidation of the heat slug 40. The solder film 30 is formed of a metal alloy which includes Pb, Sn, Ag, In and/or Bi. Such metal alloy typically has thermal conductivity of 25W/mK to 40W/mK and good adhesion strength. The solder film 30 preferably has a size equal to or greater than that of the semiconductor chip 10, so that the solder film 30 covers the whole backside of the chip 20. The adhesion layer 14, which promotes the adhesion between the semiconductor chip 10 and the solder film 30, typically has a multi-layer metal structure. Exemplary structures of the layer 14 include VNi/Au, Ti/VNi/Au, Cr/VNi/Au, Ti/Pt/Au, Cr/CrCu/(Cu)/Au, TiW/(Cu, NiV)/Au, VNi/Pd, Ti/VNi/Pd, Cr/VNi/Pd, Ti/Pt/Pd, Cr/CrCu/(Cu)/Pd, and TiW/(Cu, NiV)/Pd.

cont. A4

Please replace the paragraph starting on page 5, line 30 with the following replacement paragraph.

In preparing the semiconductor chip 10 of FIG. 4A, the under-bump metallurgy (UBM) layer 17, which includes Cr, Cr/Cu, and Cu layers, is formed on the chip pads (not shown) of the semiconductor substrate 11, in and on which circuits (not shown) have been formed, by known sputtering and patterning. Typically, the semiconductor substrate 11 is a silicon wafer. On the patterned UBM layer 17, under which the chip pads are, the conductive bumps 16 are formed. Then, the adhesion layer 14 is formed on the backside of the semiconductor substrate 11 by sputtering, evaporation, electro-plating, or electroless-plating. As previously described, the metal layer 14 is formed of a multi-layer metal film such as VNi/Au, Ti/VNi/Au, Cr/VNi/Au, Ti/Pt/Au, Cr/CrCu/(Cu)/Au, TiW/(Cu, NiV)/Au, VNi/Pd, Ti/VNi/Pd, Cr/VNi/Pd, Ti/Pt/Pd, Cr/CrCu/(Cu)/Pd, or TiW/(Cu, NiV)/Pd.

A5

Please replace the paragraph starting on page 6, line 11 with the following replacement paragraph.

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A6

Before the forming of the adhesion layer 14, the backside of the semiconductor substrate 11 can be chemically cleaned using an HF solution to strengthen the bonding

cont. A6

between the semiconductor substrate 11 and the adhesion layer 14. The cleaning process can be carried out by plasma cleaning.

Please replace the paragraph starting on page 6, line 16 with the following replacement paragraph.

A7

The formation of the UBM layer 17 and the conductive bump 16, and the formation of the adhesion layer 14 can be performed in a reverse order. After the formation of UBM layer 17, the conductive bump 16, and adhesion layer 14, the semiconductor substrate in a wafer form is divided into multiple pieces of semiconductor chips 10 by sawing process.

Please replace the paragraph starting on page 6, line 21 with the following replacement paragraph.

A8

Referring to FIG. 4B, in order to attach the heat slug 40 to the backside of the semiconductor chip 10, a bonding apparatus (not shown) aligns the heat slug 40 and the solder film 30 on the backside of the semiconductor chip 10, and applies heat to the aligned elements under H_2 environment. The heat application medium can be a furnace or a thermode pressing the heat slug 40 from the top.

Please replace the paragraph starting on page 6, line 27 with the following replacement paragraph.

A9

Referring to FIG. 4C, the semiconductor chip 10 with the heat slug 40 attached thereon is attached to the substrate 20. The semiconductor chip 10 is placed on the substrate 20 with the conductive bumps 16 of the semiconductor chip 10 on respective bonding pads of the substrate 20. Then, heating in a reflow furnace attaches the semiconductor chip 10 to the substrate 20. Alternatively, an adhesive layer (not shown), which bonds the conductive bumps 17 to the respective bonding pads 22, attaches the semiconductor chip 10 to the substrate 20. After the bonding between the conductive bumps 17 and the respective bonding pads 22, liquid resin is injected into the space between the semiconductor chip 10 and the substrate 20 to form the under-filling portion 50. Accordingly, the semiconductor package 100 has been completed.

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